

FIGURE 1 (PRIOR ART)

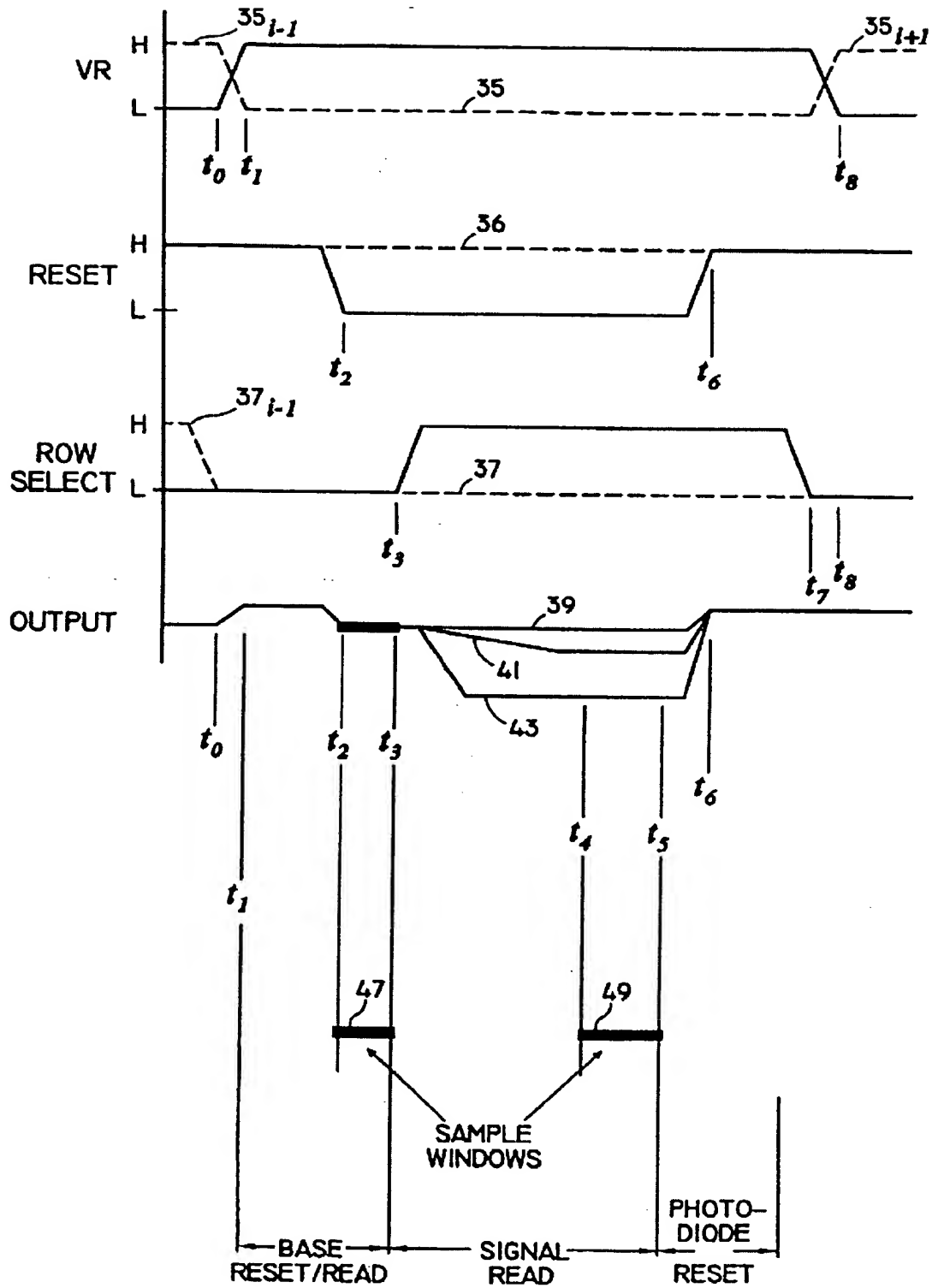


FIGURE 2 (PRIOR ART)

009201" E026960

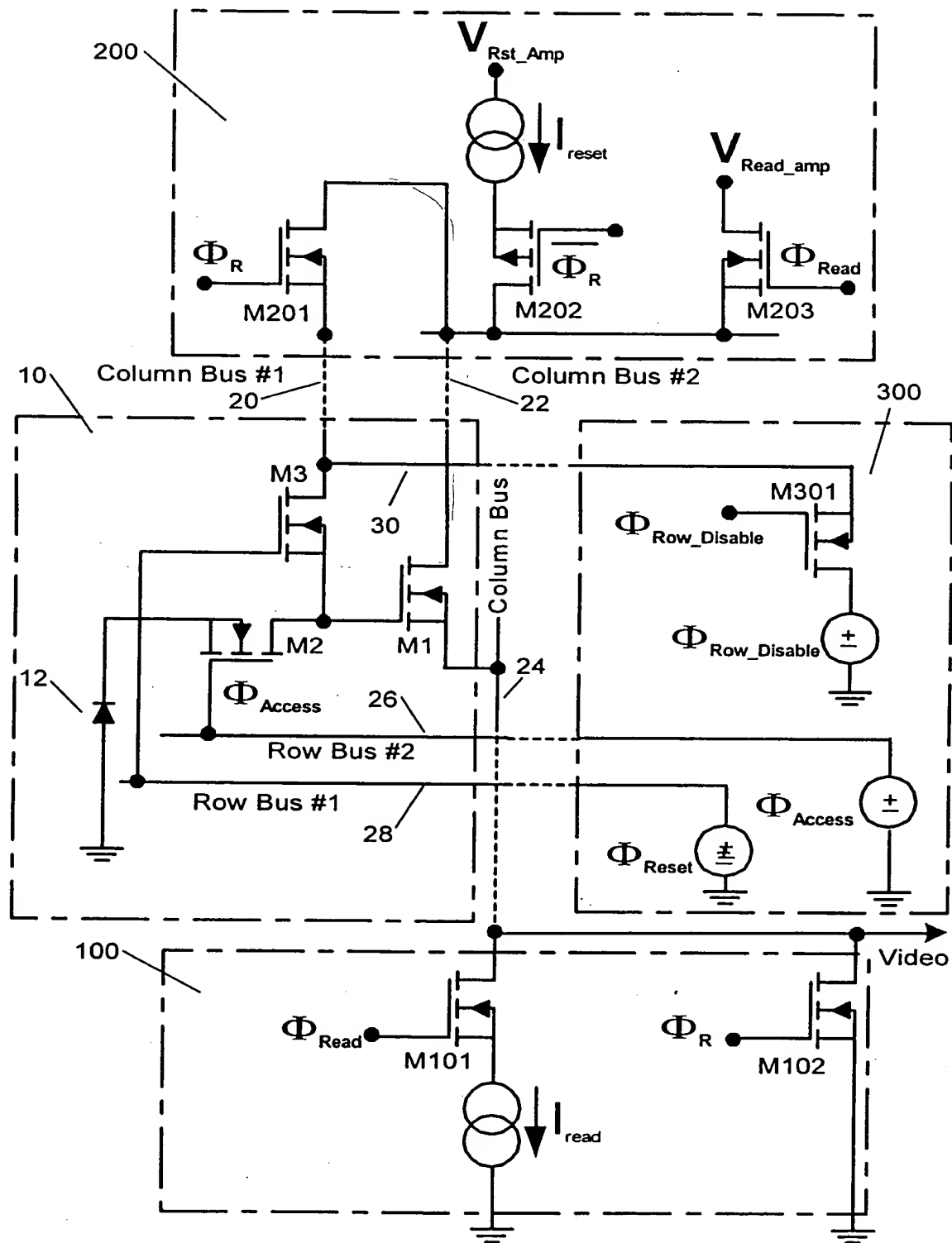


FIGURE 3

009201 E026950

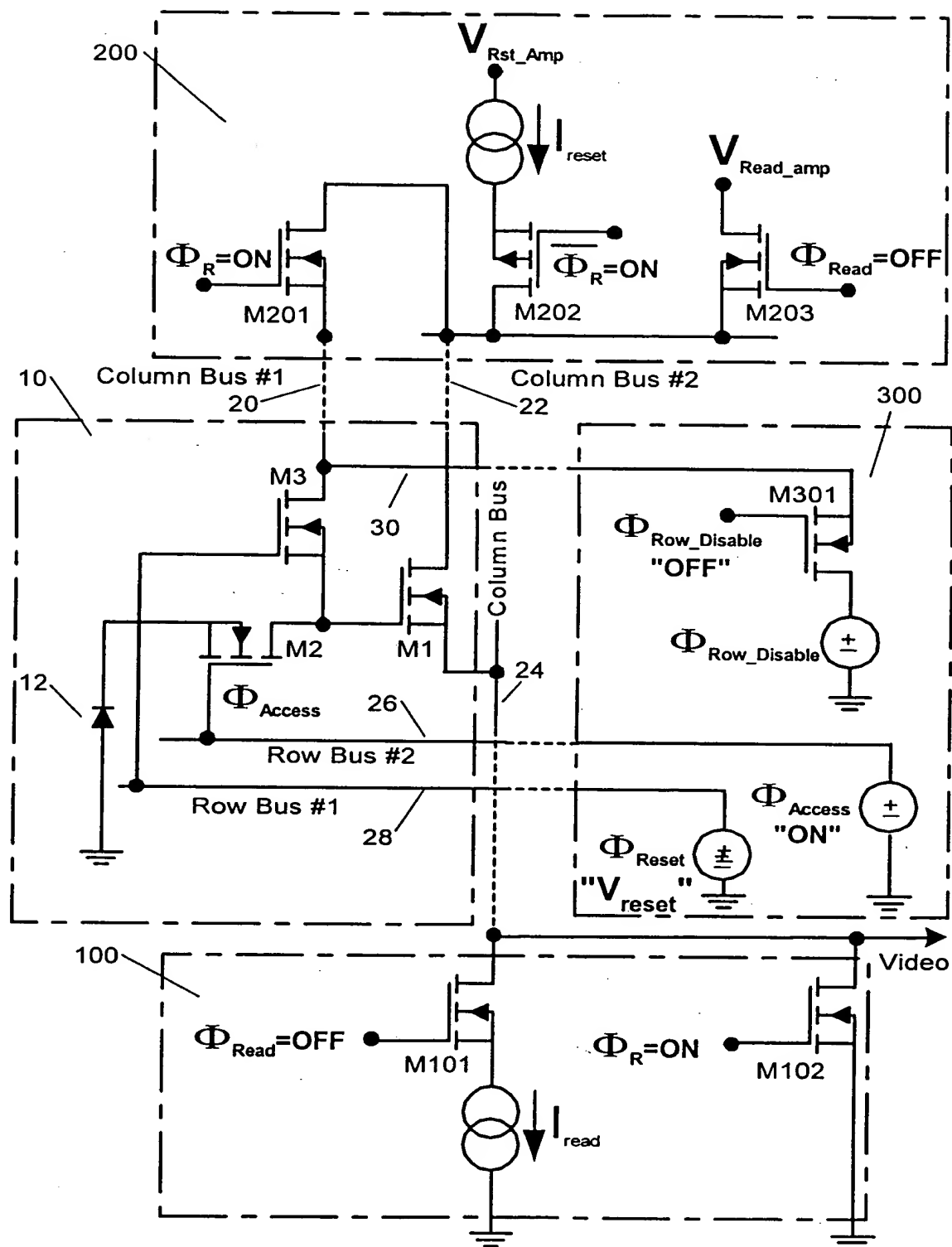


FIGURE 4 (RESET)

The schematic diagram illustrates a video signal processing circuit, divided into three main functional blocks: 100, 200, and 300.

- Block 100 (Bottom):** This block contains two transistors, M101 and M102, both controlled by  $\Phi_{Read} = OFF$ . They are connected to a common output line labeled "Video". A current source  $I_{read}$  is connected to the gates of these transistors.
- Block 200 (Top):** This block contains three transistors, M201, M202, and M203, all controlled by  $\Phi_R = OFF$ . They are connected to a common input line. A current source  $I_{reset}$  is connected to the gates of M202 and M203. A voltage source  $V$  is connected to the gates of M201 and M202.
- Block 300 (Right):** This block contains a transistor M301 controlled by  $\Phi_{Row\_Disable} = "ON"$ . It is connected to a common input line. A voltage source  $V$  is connected to the gates of M301 and M203. A current source  $I_{reset}$  is connected to the gates of M202 and M203.

The circuit also includes several buses and control signals:

- Column Buses:** Column Bus #1 (20), Column Bus #2 (22), and a central Column Bus (24).
- Row Buses:** Row Bus #1 (28) and Row Bus #2 (26).
- Control Signals:**  $\Phi_{Access}$ ,  $\Phi_{Reset} = "OFF"$ , and  $\Phi_{Access} = "OFF"$ .
- Other Components:** A diode (12) is connected to Row Bus #1. A voltage source  $V$  is connected to the gates of M201, M202, and M301. A current source  $I_{reset}$  is connected to the gates of M202 and M203.

FIGURE 5 (INTEGRATE)

The schematic diagram illustrates a video signal processing circuit, divided into three main functional blocks: 100, 200, and 300.

- Block 200 (Top):** This block contains the input and reset stages. It features two input transistors, M201 and M202, both controlled by  $\Phi_R = \text{OFF}$ . M201's source is connected to Column Bus #1 (20), and M202's source is connected to Column Bus #2 (22). Both gates are connected to a common input signal. The output of M202 is connected to a reset current source  $I_{\text{reset}}$  (represented by a circle with a downward arrow) and a voltage source  $V_{\text{Rst\_Amp}}$ . The output of M201 is connected to the input of transistor M203, which is controlled by  $\Phi_{\text{Read}} = \text{ON}$ . The source of M203 is connected to a read current source  $I_{\text{read}}$  (represented by a circle with a downward arrow) and a voltage source  $V_{\text{Read\_amp}}$ .
- Block 100 (Bottom):** This block contains the output stage. It features two output transistors, M101 and M102, both controlled by  $\Phi_R = \text{OFF}$ . M101's source is connected to the output of M203 (from Block 200), and M102's source is connected to the output of M202 (from Block 200). Both gates are connected to a common output signal. The output of M101 is connected to a read current source  $I_{\text{read}}$  (represented by a circle with a downward arrow) and a voltage source  $V_{\text{Rst\_Amp}}$ . The output of M102 is connected to a read current source  $I_{\text{read}}$  (represented by a circle with a downward arrow) and a voltage source  $V_{\text{Read\_amp}}$ .
- Block 300 (Middle):** This block contains the internal processing and control logic. It features a central Column Bus (24) and two Row Buses, Row Bus #1 (28) and Row Bus #2 (26). Transistors M1, M2, and M3 are connected to the Column Bus. M1 and M2 are controlled by  $\Phi_{\text{Access}}$ , and M3 is controlled by  $\Phi_{\text{Row\_Disable}} = \text{"OFF"}$ . The output of M3 is connected to a voltage source  $V_{\text{Rst\_Amp}}$ . The output of M1 is connected to a read current source  $I_{\text{read}}$  (represented by a circle with a downward arrow) and a voltage source  $V_{\text{Read\_amp}}$ . The output of M2 is connected to a read current source  $I_{\text{read}}$  (represented by a circle with a downward arrow) and a voltage source  $V_{\text{Read\_amp}}$ . The output of M3 is connected to a read current source  $I_{\text{read}}$  (represented by a circle with a downward arrow) and a voltage source  $V_{\text{Read\_amp}}$ . The output of M1 is connected to a read current source  $I_{\text{read}}$  (represented by a circle with a downward arrow) and a voltage source  $V_{\text{Read\_amp}}$ . The output of M2 is connected to a read current source  $I_{\text{read}}$  (represented by a circle with a downward arrow) and a voltage source  $V_{\text{Read\_amp}}$ . The output of M3 is connected to a read current source  $I_{\text{read}}$  (represented by a circle with a downward arrow) and a voltage source  $V_{\text{Read\_amp}}$ .

FIGURE 6 (READ)

00920T" E0279960

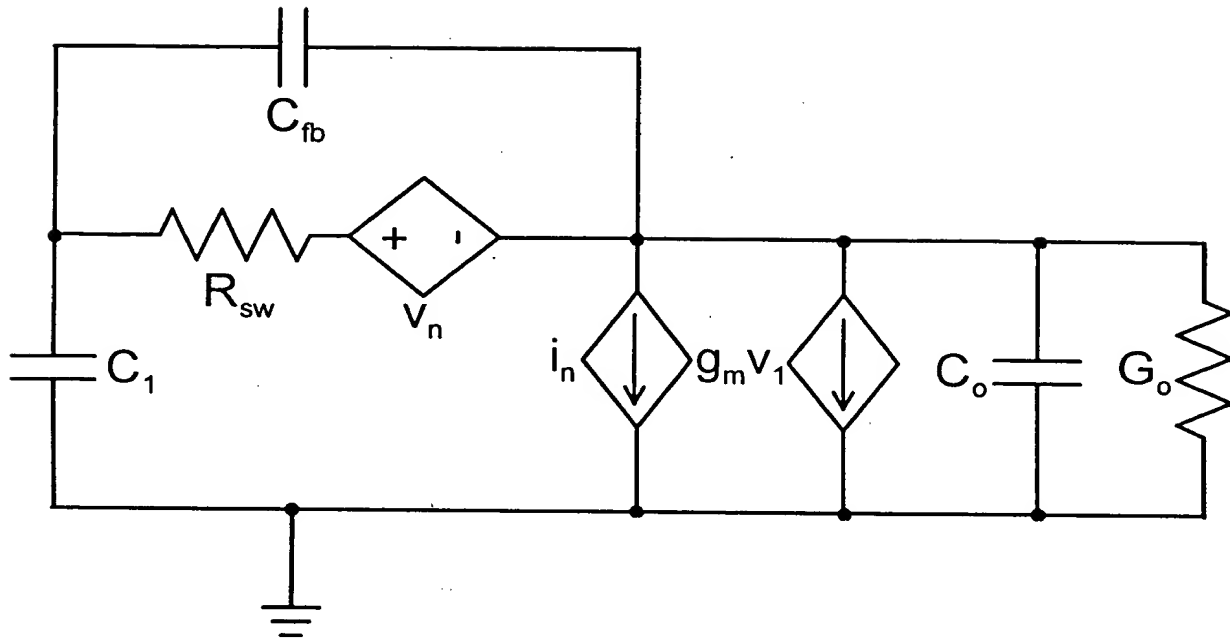


FIGURE 7

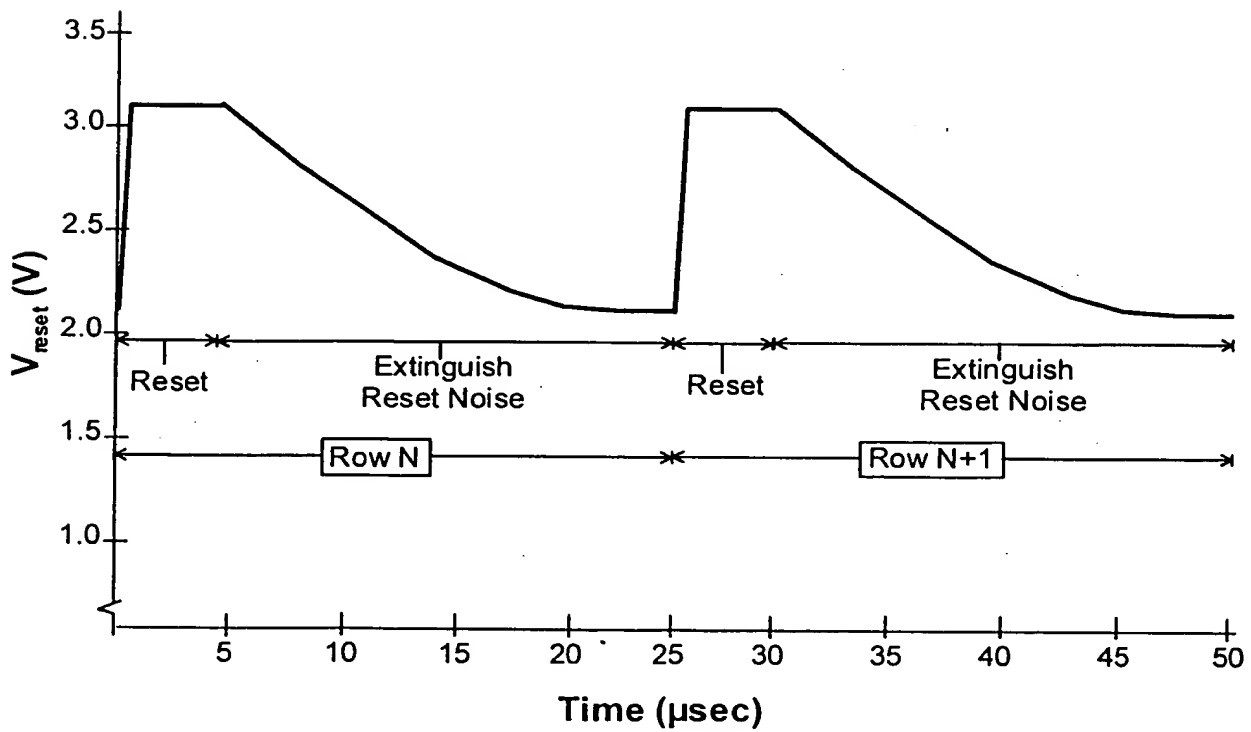
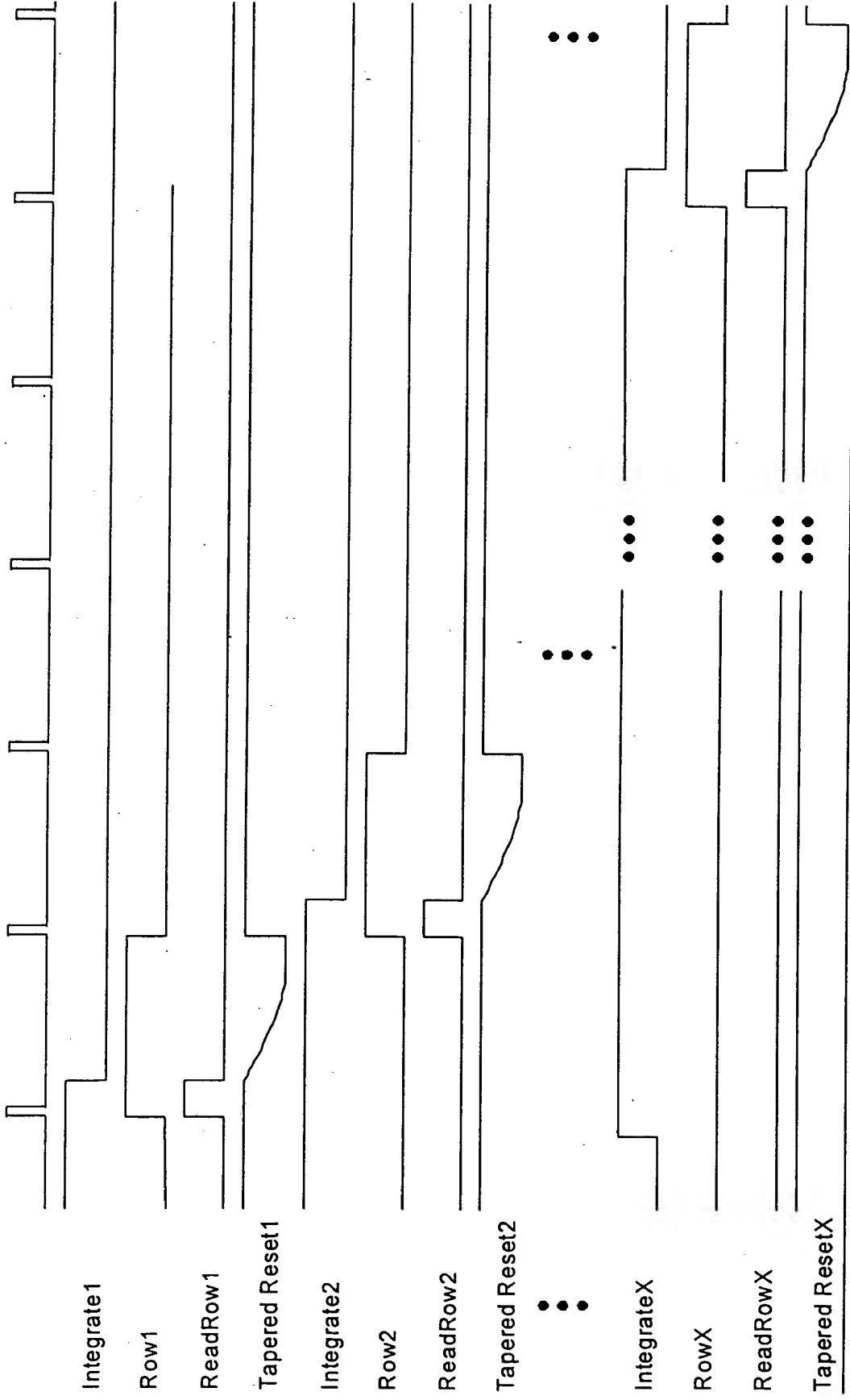


FIGURE 8

*Representative Timing Diagram for X by Y CMOS Imager*



**FIGURE 9**